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09/624,718	07/25/2000	Shinichi Yoshimura	112857-062	6804

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BELL, BOYD & LLOYD, LLC
P. O. BOX 1135
CHICAGO, IL 60690-1135

EXAMINER	
KAO, CHIH CHENG G	

ART UNIT	PAPER NUMBER
2882	

DATE MAILED: 10/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/624,718	YOSHIMURA, SHINICHI	
	Examiner	Art Unit	
	Chih-Cheng Glen Kao	2882	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2000 and 17 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *17* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected drawings were received on 7/17/03. These drawings are objected to because a typographical error still appears to exist on Figure 5: "k+3" and "k+2" in the wrong positions on the graph. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1-3, 5, 6, 10, and 13-15 are objected to because of the following informalities, which appear to be minor draft errors creating lack of antecedent basis or grammatical problems: (claim 1, line 6, "for corresponding one of said elements"), (claim 1, line 7, "said operating means"), (claim 1, line 13, "said outputting means"), (claim 2, line 2, "said operation means"), (claim 3, line 2, "said operation means"), (claim 5, line 2, "said outputting means"), (claim 5, lines 2-3, "the rows or the columns"), (claim 6, line 7, "of the processing"), (claim 6, line 14, "the processing"), (claim 10, line 2, "the outputting means"), (claim 10, lines 2-3, "the rows or the columns"), (claim 13, lines 1-2, "said operation means"), (claim 14, lines 1-2, "said operation means"), and (claim 15, lines 1-2, "said operation means").

The following respective suggestions may obviate the objections: (claim 1, line 6, inserting - -a- - before "corresponding"), (claim 1, line 7, replacing "means" with - -units- -), (claim 1, line 13, replacing "means" with - -units- -), (claim 2, line 2, replacing "operation

means" with - -operating units- -), (claim 3, line 2, replacing "operation means" with - -operating units- -), (claim 5, line 2, replacing "means" with - -units- -), (claim 5, lines 2-3, inserting - -of rows and columns- - after "matrix" in claim 1, line 2), (claim 6, line 7, deleting "of the processing"), (claim 6, line 14, deleting "the"), (claim 10, line 2, replacing "means" with - -units- -), (claim 10, lines 1-2, inserting - -of rows and columns- - after "matrix" in claim 6, line 2), (claim 13, lines 1-2, replacing "operation means" with - -operating units- -), (claim 14, lines 1-2, replacing "operation means" with - -operating units- -), and (claim 15, lines 1-2, replacing "operation means" with - -operating units- -).

For purpose of examination, the claims have been treated as such. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kochi et al. (US patent 6166583) in view of Ogawa et al. (US Patent 5926057).

4. Regarding claims 1 and 6, Kochi et al. discloses an image processing apparatus and a substantially similar method having an optical area in which a plurality of elements are disposed in a matrix (Fig. 19A), comprising: light reception means (Fig. 19A, #60); arithmetic operation

means for arithmetically operating a signal obtained for each of said elements by the photoelectric conversion by said light reception means by a predetermined rule (Fig. 19A, #50); and outputting means for outputting a result of the arithmetic operation of said arithmetic operation means for each of said elements (Fig. 19A, output from #50).

However Kochi et al. does not disclose "timing adjustment means for adjusting a timing at which the result of the arithmetic operation is to be outputted for each of said plurality of elements from said outputting means" in this embodiment, operation of operating means based on at least one of a clear signal and transfer signal with outputting means in this embodiment, timing adjustment or modes using a control signal other than the clear or transfer signal in this embodiment, nor a plurality of operating and outputting units.

Kochi et al. further teaches timing adjustment means for adjusting a timing at which the result of the arithmetic operation is to be outputted for each of said plurality of elements from said outputting means (Fig. 12, and col. 11, lines 9-12) in another embodiment. Kochi et al. further teaches operation of operating means based on at least one of a clear signal and transfer signal with outputting means (col. 8, lines 57-60). Kochi et al. further teaches timing adjustment or modes using a control signal other than the clear or transfer signal (col. 4, lines 59-67) in another embodiment. Ogawa et al. implies a plurality of operating and outputting units (col. 1, lines 33-36).

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to combine the image processing apparatus and method of Kochi et al. with the timing adjustment, since one would be motivated to incorporate it to improve operation speed as suggested by Kochi et al. (col. 2, lines 5-9 and 57-58).

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to combine the suggested device of Kochi et al. with the transfer signal for the operation means with outputting means, since one would be motivated to use it for transferring signals to an output as implied from Kochi et al. (col. 8, lines 57-60).

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to combine the suggested device of Kochi et al. with the control signal for the timing adjustment or modes, since one would be motivated to use it for control of latch circuits and timing as implied by Kochi et al. (col. 4, lines 59-67, and col. 11, lines 9-13).

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to have the suggested apparatus and method of Kochi et al. with the plurality of operating and outputting units of Ogawa et al., since one would be motivated to incorporate this for faster processing (col. 1, lines 33-36) as implied from Ogawa et al.

5. Regarding claims 2 and 7, Kochi et al. in view of Ogawa et al. suggests a method and apparatus as recited above.

However, Kochi et al. does not disclose wherein said arithmetic operation means and a substantially similar step includes storage means for successively storing a plurality of signals at different timings obtained by the photoelectric conversion.

Kochi et al. further teaches storage means for successively storing a plurality of signals at different timings obtained by the photoelectric conversion (Fig. 19A, #43 and 45).

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to have the suggested apparatus and method of Kochi et al. in view of

Ogawa et al. with the arithmetic operation means and step including the storage means, since rearranging parts of an invention and forming in one piece a component which has formerly been formed in two elements and put together only involves only routine skill in the art. One would be motivated to rearrange and integrate the components to prevent or minimize an increase in circuit scale as suggested by Kochi et al. (col. 2, lines 5-9).

6. Regarding claims 3, 4, 8, and 9, Kochi et al. in view of Ogawa et al. suggests a method and apparatus as recited above.

However, Kochi et al. does not disclose wherein said arithmetic operation means and a substantially similar step executes comparison arithmetic operation for a combination of a plurality of ones of the signals stored in said storage means, wherein the comparison arithmetic operation includes an arithmetic operation for determining a maximum value or a minimum value of the signal.

Kochi et al. further teaches means and a substantially similar step of executing comparison arithmetic operation for a combination of a plurality of ones of the signals stored in said storage means (col. 1, lines 39-42, Fig. 19A, #44 and 48, Fig. 18) and wherein the comparison arithmetic operation includes an arithmetic operation for determining a maximum value or a minimum value of the signal (Fig. 18, #66).

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to have the suggested apparatus and method of Kochi et al. in view of Ogawa et al. with the arithmetic operation means and step including the comparison arithmetic operation and determination of a maximum or minimum value, since rearranging parts of an

invention and forming in one piece a component which has formerly been formed in two elements and put together only involves only routine skill in the art. One would be motivated to rearrange and integrate the components to prevent or minimize an increase in circuit scale as suggested by Kochi et al. (col. 2, lines 5-9).

7. Regarding claims 5 and 10, Kochi et al. in view of Ogawa et al. suggests a method and apparatus as recited above.

However, Kochi et al. does not disclose outputting means and a substantially similar step outputting results of the arithmetic operation for each of the rows or the columns of said elements at a timing adjusted by said timing adjustment means.

Kochi et al. further teaches wherein said outputting means and a substantially similar step outputting results of the arithmetic operation for each of the rows or the columns of said elements at a timing adjusted by said timing adjustment means (Fig. 18, and col. 11, lines 10-13).

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to have the suggested apparatus and method of Kochi et al. in view of Ogawa et al. with outputting means at a timing adjusted by said timing adjustment means, since rearranging parts of an invention and forming in one piece a component which has formerly been formed in two elements and put together only involves only routine skill in the art. One would be motivated to rearrange and integrate the components to prevent or minimize an increase in circuit scale as suggested by Kochi et al. (col. 2, lines 5-9).

8. Regarding claims 11 and 12, Kochi et al. in view of Ogawa et al. suggests a method and apparatus as recited above.

However, Kochi et al. does not disclose a plurality of modes represented by different expressions from each other.

Ogawa et al. implies a plurality of modes represented by different expressions from each other (col. 3, lines 32-38).

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to have the suggested apparatus and method of Kochi et al. in view of Ogawa et al. with the plurality of modes, since one would be motivated to incorporate this for more functions as implied from Ogawa et al. (col. 1, lines 32-38).

9. With regards to claim 13, Kochi et al. further discloses arithmetic operations (Fig. 19A, #50).

10. With regards to claims 14 and 15, Kochi et al. in view of Ogawa et al. suggests a method and apparatus as recited above.

However, Kochi et al. does not disclose operation means storing and operating at predetermined timing intervals in the order in which signals are received in this embodiment.

Kochi et al. further teaches operation means storing and operating at predetermined timing intervals in another embodiment in the order in which signals are received (Figs. 16A-16G).

It would have been obvious, to one having ordinary skill in the art at the time the invention was made, to have the suggested apparatus and method of Kochi et al. in view of Ogawa et al. with the timing intervals, since one would be motivated to incorporate it to repetitively process signals as implied from Kochi et al. (Fig. 16A-16G).

Response to Arguments

11. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Parallel processing by using a plurality of chips that have the same function, but for different elements, as implied from claim 1 of the instant application, is known in the art as implied from Ogawa et al. (col. 1, lines 33-36). Although there may be a disadvantage of increased chip area due to the multitude of components, the advantages and motivations for use lie in increased processor speed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chih-Cheng Glen Kao whose telephone number is (703) 605-5298. The examiner can normally be reached on M - F (9 am to 5 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ed Glick can be reached on (703) 308-4858. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

gk

DAVID V. BRUCE
PRIMARY EXAMINER